

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#10/B  
4-19-02  
AJONES

Applicant: Donald Craig Foster  
Assignee: Amkor Technology, Inc.  
Title: Stackable Lead Frame Package Using Exposed Internal Lead Traces  
Serial No.: 09/829,341 ✓ Filing Date: April 9, 2001  
Examiner: Tuan T. Dinh Group Art Unit: 2827  
Docket No.: M-9950 US



San Jose, California  
April 8, 2002

COMMISSIONER FOR PATENTS  
Washington, D. C. 20231

**RESPONSE TO OFFICE ACTION MAILED MARCH 12, 2002**

Dear Sir:

Applicant responds to the Office Action mailed March 12, 2002 as follows

**IN THE SPECIFICATION**

Please amend the Specification by replacing the paragraphs listed below with the indicated replacement paragraph. An appendix hereto, entitled Version with Markings to Show Changes Made, shows the changes being made to the particular paragraphs.

Please replace the paragraph beginning on page 4, line 9 with the following paragraph.

Fig. 1 is a top view of a lead frame for use in forming internal leads.

Please replace the paragraph beginning on page 4, line 11 with the following paragraph.

Fig. 2 shows a lead frame with internal leads formed from the lead frame of Fig. 1.

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Please replace the paragraph beginning on page 4, line 23 with the following paragraph.

B<sub>3</sub>

Figs. 7A and 7B are top views of a partial lead frame, according to another embodiment of the present invention, in which the external and internal leads are interleaved.

Please replace the paragraph beginning on page 4, line 27 with the following paragraph.

B<sub>4</sub>

Fig. 8 is a side view of a portion of a die package utilizing the lead frame of Fig. 7B.

Please replace the paragraph beginning on page 5, line 20 with the following paragraph.

B<sub>5</sub>

Fig. 1 is a top view of an ILT lead frame 10 having a plurality of first external lead fingers or outer lead traces (OLTs) 12 and an internal paddle area 14 containing slots 16 and traces 17, where traces 17 are electrically connected. Lead frame 10 is shown having slots 16 ending at three sides of the package. However, the lead frame can be any suitable type, such as for a dual-sided or quad package.

Please replace the paragraph beginning on page 6, line 13 with the following paragraph.

B<sub>6</sub>

Fig. 2 shows lead frame 10 after removal of the outer portions of paddle area 14. Traces 17 are no longer electrically connected to other traces. Instead, each resulting inner lead trace 20 is electrically isolated from other ILTs 20. As shown in Fig. 2, ILTs 20 can carry signals to and from adjacent sides or to and from opposite sides of paddle area 14. It should be noted that the lead frame shown in Fig. 2 can be modified so that ILTs 20 can carry signals to and from the perimeter and the interior of paddle area 14 for die with center bond

B6  
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pads. To achieve this, an interior portion of paddle area 14 is removed, such that ILTs 20 have ends at the perimeter and interior of paddle area 14. This is in contrast to lead frame 10 of Fig. 2, in which ILTs 20 have ends only at the perimeter of the paddle area.

Please replace the paragraph beginning on page 6, line 29 with the following paragraph.

B7

A die can then be attached to lead frame 10 of Fig. 2. Fig. 3A is a side view of a lead frame package 10-1 with a die 30, according to one embodiment. Die 30 is secured to ILTs 20 using a non-conductive film or die attach paste 32, with an inner lead trace (ILT) tape 33, such as a standard lead locking tape discussed above, placed on the bottom of ILT 20. Note that die 30 may also be secured to ILT tape 33 by film or paste 32 when tape 33 is placed on top of ILTs 20 (see Fig. 3B). The ends of ILTs 20 are down set or bent, such that the ends will be exposed after die 10 has been encapsulated or packaged, such as with a conventional encapsulant or mold compound 34. The position of ILTs 20 can be on approximately the same plane as the external lead bond fingers, the die attach pad, or somewhere in between. The ends of ILTs 20 are down set during the manufacture of the lead frame, prior to the die assembly process. Bond pads 36 of die 30 and selected ones of ILTs 20 and OLTs 12 are wire-bonded, such as with thin conductive bond wires 35, to provide the desired signal routing or interconnections between the die and the ILTs and OLTs. The package can then be encased, such as with encapsulant or mold compound 34. Portions of OLTs 12 and ILTs 20 are then attached to a printed circuit board (PCB) 37, such as with solder 38, to provide electrical connection between PCB 37 and die 30, via OLTs 12 and ILTs 20. Consequently, an increased number of inputs and outputs are possible to and from die 30.

Please replace the paragraph beginning on page 7, line 26 with the following paragraph.

B<sub>8</sub>

Fig. 3B is a side view of another embodiment of a lead frame package 10-2 with die 30. As noted above, die 30 is secured to ILT tape 33 by non-conductive film or paste 32 when tape 33 is placed on top of ILTs 20. In this embodiment, interior portions of ILTs 20 are also exposed through encapsulant 34, such as through an ILT pad 39. Die 30 can then be electrically connected to PCB 37 through OLTs 12, ILTs 20, and ILT pad 39 and solder 38. The additional connection using ILT pad 39 helps solve high frequency applications by creating low inductance signal paths through the bottom exposed ILT leads, with the exposed pad handling increased thermal needs due to the high frequency.

Please replace the paragraph beginning on page 8, line 7 with the following paragraph.

B<sub>9</sub>

Fig. 4 is a top view showing one configuration and pattern of OLTs 12 and ILTs 20 electrically connected to die 30 in a lead frame package 10-3. Note that only the outline of die 30 is shown to illustrate the underlying ILTs 20.

Please replace the paragraph beginning on page 8, line 11 with the following paragraph.

B<sub>10</sub>

In another embodiment, ILTs 20 can be down set or bent away from OLTs 12, as shown in lead frame package 10-4 of Fig. 5. In this embodiment, ILTs 20 are exposed on the upper surface of the die package. As shown in Fig. 6, this allows a second die package 60 to be stacked and electrically connected to die 30. External leads or fingers 62 from second die package 60 can be attached to ILTs 20 with a conductive material, such as solder 64. Connections from both die 30 and a die 66 of second die package 60 to PCB 37 are available through OLTs 12 and solder 38. As a result, multiple die and packages can be stacked and connected, and with thin package design, having a lower profile than conventional packages. Further, individual die in each package can first be tested before the die and package are

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stacked and connected to another die. If the die is bad or non-functioning, it is not connected to good die, thereby preventing bad die from consuming good die. Consequently, yield is increased over conventional single packages with stacked multiple die.

Please replace the paragraph beginning on page 8, line 31 with the following paragraph.

B11

Other embodiments of the present invention utilize ILTs and OLTs that are interleaved. This is in contrast to the above embodiments, in which the ends of the ILTs and OLTs do not overlap, i.e., not interleaved. Fig. 7A shows a portion of a partially-complete lead frame 11 having external leads 70 and internal leads 72. Internal leads 72 are exposed above dotted line 74, underneath which indicates the ILT tape. As seen from Fig. 7A, external leads 70 and internal leads 72 are electrically connected at portions 76 prior to trimming according to allow conventional lead frame manufacturing process. Fig. 7B shows the portion of the lead frame 11 of Fig. 7A after trimming away portions 76, where the dotted line 78 indicates the trim area. As a result, interleaved external leads 70 and internal leads 72 are electrically isolated. The ends of internal leads 72 extend beyond the ends of external leads 70, which are now closer to the die. This allows the use of shorter bonding wires between external leads 70 and the die and enables exposed ILT pads to accommodate larger package outlines for stacking on top.

Please replace the paragraph beginning on page 9, line 21 with the following paragraph.

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B12

A die can then be attached to the lead frame 11 of Fig. 7B. The die can be attached, such as described above with respect to Fig. 3 or using any other suitable processes. Fig. 8 is a side view of a portion of die 30 attached to the lead frame 11 of a package 10-5. Die 30 is

B12

affixed to the lead frame with die attach paste 32. ILT tape 33 is placed on the bottom of the internal leads 70. The ends of internal leads 70 are down set or bent, such that the ends will be exposed after die 30 has been encapsulated or packaged. The position of the ends of internal leads 70 can be on approximately the same plane as the ends of external leads 72, the die attach pad, or somewhere in between. Wire bonding then provides electrical connection between die 30 and internal leads 70 and external leads 72, such as with bond wires 35 attached to bond pads 36. Note that the bond wires connected to external leads 72 in this embodiment are shorter than with the embodiment of Fig. 3. The package 10-5 can then be encased, such as with encapsulant or mold compound 34. Thus, similar to Fig. 3, this embodiment provides additional input/output connections to die 30.

Please replace the paragraph beginning on page 10, line 11 with the following paragraph.

B13

Fig. 9 is a top view showing one embodiment of a lead frame package 10-6 the invention, in which external leads 72 and internal leads 70 are interleaved. Note that bond wires 35 connected to external leads 72 are shorter here than the corresponding bond wires 35 of Fig. 4.

Please replace the paragraph beginning on page 10, line 16 with the following paragraph.

B14

In another embodiment, Fig. 10 is a side view of a portion of a lead frame package 10-7, in which internal leads 70 have been down set or bent away from external leads 72, similar to Fig. 5 above. Internal leads 70 are exposed on the upper surface of the die package, thereby allowing a second die package to be electrically connected thereto, similar to Fig. 6 above. Again, the difference with this embodiment is shorter bond wires between the die and

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the external leads and a larger package outline for stacking on top can be accommodated.

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IN THE CLAIMS

Please amend claims 2, 3, 39, 41, and 42 as shown in the Appendix hereto. Below is a list of all of the now pending claims.

1. A semiconductor die package, comprising:  
conductive outer leads having first ends extending outside the package and second ends extending toward the interior of the package;  
conductive inner leads having first ends extending to and electrically accessible through a first surface of the package; and  
a first die electrically connected to the inner and outer leads.

2. (Amended) The package of Claim 1, wherein the second ends of the outer leads do not extend beyond the first ends of the inner leads.

3. (Amended) The package of Claim 1, wherein the second ends of the outer leads extend beyond the first ends of the inner leads.

4. The package of Claim 1, wherein the first surface is a bottom surface.

5. The package of Claim 4, further comprising a printed circuit board electrically coupled to the outer and inner leads.

6. The package of Claim 4, wherein the first ends of the inner leads are approximately co-planar with the first ends of the outer leads.

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7. The package of Claim 4, wherein the first die is positioned above the inner leads.

8. The package of Claim 1, wherein the first surface is an upper surface.

9. The package of Claim 8, wherein the first die is positioned between the outer leads and the inner leads.

10. The package of Claim 8, further comprising a second semiconductor die package coupled to the first die, wherein the second semiconductor die package comprises a second die and outer leads coupled to the second die.

11. The package of Claim 10, wherein the outer leads of the second die are electrically coupled to the inner leads of the first die.

12. The package of Claim 11, wherein the second die package is positioned over the first die.

13. The package of Claim 1, wherein the inner leads further comprise an interior portion electrically accessible through the first surface, and wherein the die is further electrically coupled to the interior portion.

14. The package of Claim 13, wherein the interior portion and the first ends of the inner leads and the first ends of the outer leads are electrically coupled to a printed circuit board.

33. The package of Claim 1, wherein the conductive inner leads are formed from an internal paddle area.

34. The package of Claim 33, further comprising means for securing and electrically isolating the conductive inner leads.

35. The package of Claim 33, wherein the first die is attached to the internal paddle area.

36. The package of Claim 33, wherein the first ends of the inner leads are closer to the die than the first ends of the outer leads.

37. The package of Claim 33, wherein the first ends of the inner leads extend beyond the second ends of the outer leads.

38. The package of Claim 33, wherein the first ends of the inner leads do not extend beyond the second ends of the outer leads.

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39. (Amended) A semiconductor die package, comprising:  
  
a lead frame having external leads;  
  
internal leads electrically isolated from the external leads and secured to the lead frame;  
  
means for securing and electrically isolating the internal leads from each other;  
  
a die electrically coupled to the external leads and the internal leads; and

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means for encapsulating the die and portions of the internal and external leads, wherein a first end of at least some of the internal leads is exposed through a surface of the means for encapsulating.

40. The package of Claim 39, wherein the internal leads are formed from an internal paddle area.

B<sub>18</sub>

41. The package of Claim 40, wherein the first ends of the internal leads are exposed through a bottom surface of the means for encapsulating.

42. The package of Claim 40, wherein the first ends of the internal leads are exposed through a top surface of the means for encapsulating.

43. The package of Claim 42, further comprising a second die package overlying the die package and electrically coupled to the internal leads of the die contained within the die package.

44. The package of Claim 40, wherein the ends of the internal leads are bent towards the surface of the means for coupling.

45. The package of Claim 40, wherein the external leads have first ends extending outside the means for encapsulating and second ends extending toward the die, and wherein the second ends of the external leads extend beyond the ends of the internal leads.

46. A semiconductor die package, comprising:

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a die;

an enclosure protecting the die;

external leads each having a first and a second end, wherein the first ends extend beyond the enclosure and the second ends are electrically coupled to the die; and

internal leads having at least first ends exposed through the enclosure, wherein the die is electrically coupled to the internal leads, and wherein the internal leads are electrically isolated from the external leads.

47. The package of Claim 46, wherein the first ends of the internal and external leads are approximately co-planar.

48. The package of Claim 46, where the first ends of the internal and external leads are located on opposite sides of the enclosure.

49. The package of Claim 48, further comprising a second die located over the die and electrically coupled to the first ends of the internal leads.

50. The package of Claim 46, wherein the first ends of the internal leads and the second ends of the external leads are interleaved.

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## REMARKS

The specification is amended to correct obvious errors, and add reference numbers to more closely tie the description to the drawings. No new matter is added.

The drawings are amended by way of a separate paper to match the changes to the specification.

Claims 2, 3, 39, 41 and 42 are amended for purposes of clarity, or to correct minor errors.

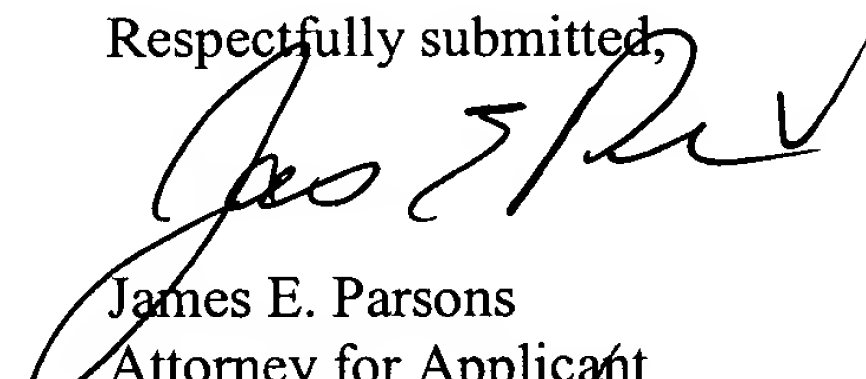
With respect to the election requirement, Applicant elects Embodiment III, as exemplified by Figure 3B. Applicant submits that claims 1, 2, 4-7, 13, 14, 33-36, 38-41, 46 and 47 are readable on Embodiment III.

Please direct any comments or questions concerning the Office Action to the undersigned at (408) 487-1315.

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Respectfully submitted,



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